REMARKS

The Examiner is thanked for the thorough examination of the present application. The Office Action, however, rejected all claims 1-17 under 35 U.S.C. § 103(a) as allegedly unpatentable over the combination of Jeddeloh (U.S. patent 6,202,133) in view of Merkey (U.S. published application 2003/0070043 A1). For at least the reasons that follow, Applicants respectfully disagree.

Discussion of Rejections

The Office Action rejected independent claims 1, 9, and 16 as allegedly obvious over the combination of Jeddeolh in view of Merkey. Independent claims 1, 9, and 16, respectively recite:

> 1. A memory system comprising:
> a host integrated circuit;
> a first memory controller having at least one associated memory defining a first address space;
> a second memory controller having at least one associated memory defining a second address space;
> ***a parity memory for storing parity information associated with data stored in the memories associated with the first and second memory controllers; and***
> ***a controller for the storing data in the parity memory, the controller configured to store parity data associated with data stored in the memory associated with the first memory controller in an interleaved fashion with data stored in the memory associated with the second memory controller.***
>
> 9. A memory system comprising:
> first data memory coupled to a first memory controller;
> second data memory coupled to a second memory controller;
> ***a parity memory coupled to a parity controller, the parity controller being directly coupled to both the first memory controller and the second memory controller;***
> ***parity data control logic configured to store and retrieve parity information associated with data stored in both the first data memory and the second data memory, the parity data control logic configured to interleave within the parity memory parity data associated with data stored in the first data memory with parity data associated with data stored in the second data memory.***

16. A method for managing parity information associated with a plurality of memory controllers comprising:

generating first parity information associated with data to be stored in a first data memory coupled to a first memory controller;

generating second parity information associated with data to be stored in a second data memory coupled to a second memory controller;

storing the first and second parity information in a parity memory coupled to a parity controller, the first and second parity information being stored in an interleaved fashion within the parity memory.

(*Emphasis added*). Applicants respectfully submit that independent claims 1, 9, and 16 patently define over the cited art of record for at least the reason that the cited art fails to disclose the features emphasized above.

With regard to the features that are emphasized above, the Office Action admitted that these features are not disclosed anywhere in the principal reference Jeddeloh. Instead, the Office Action relies on teachings from Merkey as disclosing the emphasized features. With regard to claim 1, these features include the claimed "parity memory ..." and "controller ..." Specifically, the Office Action cited reference numeral 226 and paragraph 73 as disclosing the claimed "parity memory for storing parity information associated with data stored in the memories associated with the first and second memory controllers." Then, the Office Action relied on paragraphs 73 and 74 or Merkey as allegedly disclosing the claimed "controller for the storing data in the parity memory, the controller configured to store parity data associated with data stored in the memory associated with the first memory controller in an interleaved fashion with data stored in the memory associated with the second memory controller." Applicants respectfully traverse this application of Merkey. In this regard, paragraphs 73 and 74 of Merkey are referring to two different types of RAID memories. Paragraph 73 refers to a RAID-4 system, while paragraph 74 refers to a RAID-5 system. Specifically, these paragraphs of Merkey state:

[0073] RAID-4 systems are similar to RAID-0 systems, in that data is striped over multiple drives, as exemplified by the three disk RAID-4 system of

> FIG. 2d. The storage spaces of disks 222 and 224 are added together in interleaved fashion, while disk 226 contains the parity of disks 222 and 224. RAID-4 systems are unique in that they include an additional disk containing parity. For each byte of data at the same position on the striped drives, parity is computed over the bytes of all the drives and stored to the parity disk. The XOR operation is used to compute parity, providing a fast and symmetric operation that can regenerate the data of a single drive, given that the data of the remaining drives remains intact. RAID-3 systems are essentially RAID-4 systems with the data striped at byte boundaries, and for that reason RAID-3 systems are generally slower than RAID-4 systems in most applications. RAID-4 and RAID-3 systems therefore are useful to provide virtual disks with redundancy, and additionally to provide large virtual drives, both with only one additional disk drive for the parity information. They have the disadvantage that the data throughput is limited by the throughput of the drive containing the parity information, which must be accessed for every read and write operation to the array.
>
> [0074] RAID-5 systems are similar to RAID-4 systems, with the difference that the parity information is striped over all the disks with the data, as exemplified by the three disk system of FIG. 2e. Disks 228, 230, and 232 each contain data and parity in interleaved fashion. Distributing the parity data generally increases the throughput of the array as compared to a RAID-4 system. RAID-5 systems may continue to operate though one of the disks has failed. RAID-6 systems are like RAID-5 systems, except that dual parity is kept to provide for normal operation if up to the failure of two drives. An example of a RAID-6 system is shown in FIG. 2f. Disks 234, 236, 238, and 240 each contain data and two parity words labeled P and R.

As can be readily verified from the above-quoted portions of Merkey, the claimed features are not properly disclosed. Specifically, and with regard to claim 1, claim 1 defines a system having first and second memory controllers, each for controlling an associated memory. In addition a "parity memory for storing parity information associated with the data stored in the [first and second associated] memories" is defined. Finally, claim 1 defines "a controller for the storing data in the parity memory, the controller configured to store parity data associated with data stored in the memory associated with the first memory controller in an interleaved fashion with data stored in the memory associated with the second memory controller."

In contrast to these claimed features, paragraph 0074 of Merkey states that "parity information is striped over all the disks with the data, as exemplified by the three disk system of

FIG. 2e. Disks 228, 230, and 232 each contain *data and parity in interleaved fashion*." As noted above, the Office Action relies on memory 226 as being the claimed "parity memory." Significantly, there is no teaching in Merkey of parity information being interleaved in this (or any) memory. Instead, Merkey states that data and parity information are interleaved in disks 228, 230, and 232. As such, Merkey clearly fails to disclose the features expressly recited in claim 1, and for at least this reason, the rejection of that claim should be withdrawn. As claims 9 and 16 were rejected in the same paragraphs as claim 1, Applicants submit that the rejections of those independent claims should be withdrawn for the same reasons.

As claims 2-8, 10-15, and 17 each depend from independent claims 1, 9, and 16, respectively, the rejections of those claims should be withdrawn for at least the same reasons.

As a separate and independent basis for the patentability of these claims, the undersigned submits that the Office Action improperly combined select features of Merkey with Jeddeloh. In combining the teachings of these two references, the Office Action alleged that the motivation for combination would have been "a faster transaction processing (See Jeddeloh, column 5, lines 5-13). Jeddeloh states that the computer system can reduce read/write delay by storing data that are mostly read in one of the system memory module while storing data that are mostly write in the other system memory module (column 5, lines 14-27). This rationale is in conflict with well-established Federal Circuit precedent for forming such rejections.

In this regard, it is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(Emphasis added) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicants note that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to create an improved RAID memory system, as claimed by the Applicants.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in

whatever form, must nevertheless be "clear and particular." Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000). The Office Action has failed to cite any apparent disadvantage of Ladd, which would prompt the combination of select teachings of Baxter therewith.

As noted above, the Office Action cited two different portions of Jeddeloh as providing the motivation for combining Merkey. However, the cited portions of Jeddeloh have nothing to do with a parity memory, much less a controller for interleaving parity information in a parity memory. As such, there is no proper motivation for combining those select teachings of Merkey.

Simply stated, the Office Action has failed to identify a proper motivation or suggestion for combining Merkey with Jeddeloh, and as such, the Office Action is deficient and the rejections should be withdrawn.

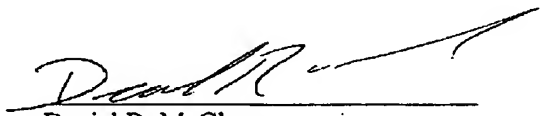
CONCLUSION

Applicant respectfully submits that all claims are in proper condition for allowance, and respectfully requests that the Examiner pass this case to issuance. If, in the opinion of the Examiner,

a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this Response to Non-Final Office Action. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to Hewlett-Packard Company's Deposit Account No. 08-2025.

Respectfully submitted,



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